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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/713,213	11/17/2003	Kenji Motomochi	L8462.03117	2453

7590 06/16/2006

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EXAMINER	
WILLIAMS, ALEXANDER O	
ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 06/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/713,213	MOTOMOCHI, KENJI	
	Examiner	Art Unit	
	Alexander O. Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/17/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Serial Number: 10/713213 Attorney's Docket #: L8462.03117
Filing Date: 11/17/2003; claimed foreign priority to 4/7/2002

Applicant: Motomochi

Examiner: Alexander Williams

Applicant's election with traverse of the species of figure 1 (claims 1 to 30), filed 4/27/06, has been acknowledged.

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the semiconductor device having a chip to chip structure wherein a first semiconductor chip having a circuit block where a plurality of inter-chip connection terminal and a plurality of external connection terminals are formed on a surface of the chip and a second semiconductor chip having a circuit block where a plurality of external connection terminals are formed on a surface of the chip are adhered to each other in a form wherein the surfaces of the chips are opposed to each other so that the inter-chip connection terminals of said first

semiconductor chip and the inter-chip connection terminals of said second semiconductor chip are connected to each other in claim 1 and similar structures in claim 23, must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claims 1 to 30 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 1 and 23, it is unclear and confusing to what is meant by and what shows "**the semiconductor device having a chip to chip structure wherein a first semiconductor chip** having a circuit block where **a plurality of inter-chip connection terminal** and **a plurality of external connection terminals** are formed on a surface of the chip **and a second semiconductor chip having a circuit block where a plurality of external connection terminals are formed on a surface of the chip are adhered to each other** in a form wherein the surfaces of the chips are opposed to each other so that the inter-chip connection terminals of said first semiconductor chip and the inter-chip connection terminals of said second semiconductor chip are connected to each other." Where is this chip on chip claimed structure shown?

Any of claims 1 to 30 not specifically addressed above are rejected as being dependent on one or more of the claims which have been specifically objected to above.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 to 30, **insofar as they can be understood**, are rejected under 35 U.S.C. § 102(e) as being anticipated by Honma et al. (U.S. Patent # 6,649,931 B2).

For example, in claim 1 and similar claim 23, Honma et al. (figures 1 to 15) specifically figures 1 and 2 show the semiconductor device having a chip **2** to chip **3** structure wherein a first semiconductor chip **2** having a circuit block (inherent, see figure 7) where a plurality of inter-chip connection terminal (inherent, see figure 6) and a plurality of external connection terminals (inherent, see figure 6) are formed on a surface of the chip and a second semiconductor chip **3** having a circuit block (inherent, see figure 7) where a plurality of external connection terminals (inherent) are formed on a surface of the chip are adhered to each other in a form wherein the surfaces of the chips are opposed to each other so that the inter-chip connection terminals of said first semiconductor chip and the inter-chip connection terminals of said second semiconductor chip are connected to each other, wherein said first semiconductor chip comprises a first multiplexer circuit (**MP**,see figure 2) for selecting an input signal line form among a plurality of input signal lines so as to output a signal from the selected input signal line to an output signal line, and the output signal line of said first multiplexer circuit is connected to an inter-chip connection terminal of said first semiconductor chip.

[0043] The semiconductor chip 2 of flash memory is composed of a memory array MA in which a plurality of memory cells are arranged like a lattice, X-system X-address buffer XAB and X-decoder XD for selecting the desired memory cells within this memory array MA, Y-axis Y-address buffer YAB and Y-decoder YD, a Y-switch/sense amplifier YS/SA for inputting and outputting data for the selected memory cells, a multiplexer MP, an input/output buffer IOB, a command user interface CUT for generating the sequence of erase/write, read mode, a write state machine WSM and a data handler DH or the like. As shown in the

figure, the memory array MA includes an ordinary memory cell area NMR, a flash fuse area FFA, an OTP area OTPA, a lock bit area LBA, an X-redundant memory cell area XRA and a Y-redundant memory cell area YRA. The areas FFA, OTPA, LBA, XRA and YRA can be selected with the commands formed through combination of the predetermined signals to be inputted to a command user interface CUT. This CUT sets selectively only one signal among the selection signals S1 to S5 to the enable state to uniquely select the areas FFA, OTPA, LBA, XRA and YRA.

[0099] The data handler DH includes the circuit block WLBI-REG and is connected to the address bus R2ADDR, data bus R2DATA and the control signal bus IOD to receive as the input signals the data of the address bus R2ADDR, data bus R2DATA and control signal bus TOD. This data handler DH is also connected to the multiplexer MP as explained above. Each circuit block within these command user interface CUI and data handler DH has the function explained below.

The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/686,685,723,724,725,728,48,678,679,296,288,529, 777,692,691,690,e25.013,e23.179,e25.011,e25.012 714/744	6/8/06
Other Documentation: foreign patents and literature in 257/686,685,723,724,725,728,48,678,679,296,288,529, 777,692,691,690,e25.013,e23.179,e25.011,e25.012 714/744	6/8/06
Electronic data base(s): U.S. Patents EAST	6/8/06

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O. Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30AM-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Alexander O Williams
Primary Examiner
Art Unit 2826

AOW
6/8/06